Amendments to the Claims

1. (currently amended): A method of making a semiconductor vertical FET device comprising the steps of:

providing a body of semiconductor material comprising a first conductivity type, wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact;

forming a first trench in the body of semiconductor material and extending from the upper surface, wherein the first trench has a first width, a first depth from the upper surface, first sidewalls, and a first bottom surface;

forming a second trench within the first trench, wherein the second trench has a second width, a second depth from the first surface, second sidewalls and a second bottom surface;

forming a first source region in the body of semiconductor material extending from the upper surface and spaced apart from the first trench; and

~~forming~~ introducing a dopant of a second conductivity type into ~~a doped gate region in~~ at least a portion of the second sidewalls and the second bottom surface to form a doped gate region, wherein the doped gate region ~~comprises a second conductivity type~~ extends into the body of semiconductor material.

2. (original): The method of claim 1 wherein the step of providing the body of semiconductor material comprises providing a III-V semiconductor substrate having a first dopant concentration and a first epitaxial layer formed on a surface of the semiconductor substrate, wherein the first epitaxial layer has a second dopant concentration less than the first dopant concentration.

3. (original): The method of claim 1 wherein the step of providing the body of semiconductor material comprises providing a body of semiconductor material comprising GaAs.

4. (currently amended): The method of claim 1 wherein the step of forming the second trench comprises the steps of:

depositing a spacer layer over the upper surface and the first trench;

etching back the ~~dielectric~~ spacer layer to form spacers that cover first sidewalls and a portion of the first bottom surface leaving a self-aligned opening in the ~~dielectric~~ spacer layer to expose a remaining portion of the bottom surface; and

etching the second trench through the opening.

5. (currently amended): The method of claim 1 wherein the step of ~~forming the doped gate region~~ introducing the dopant of the second conductivity type comprises implanting [[a]] the dopant ~~species~~ into the second sidewalls and the second bottom surface.

6. (original): The method of claim 5 wherein the step of implanting the dopant species includes implanting one of beryllium and carbon.

7. (original): The method of claim 1 further comprising the steps of:

forming a first passivation layer over the doped gate region; and

forming a second passivation layer over the first passivation layer.

8. (original): The method of claim 7, wherein the step of forming the second passivation comprises the steps of:

depositing a dielectric material over the first passivation layer; and

planarizing the dielectric material to form the second passivation layer.

9. (original): The method of claim 1 further comprising the step forming a second source region in the body of semiconductor material spaced apart from the first trench, wherein the first trench is between the first and second sources.

10. (original): The method of claim 1 wherein the step of forming the first trench includes etching the first trench using one of reactive ion etching and electron cyclotron resonance etching.

11. (original): The method of claim 1 wherein the step of forming the second trench includes etching the second trench using one of reactive ion etching and electron cyclotron resonance etching.

12. (original): A process for making a compound semiconductor vertical FET device comprising the steps of:

forming a first groove in a compound semiconductor layer of a first conductivity type, wherein the first groove has first sidewalls and a first lower surface, and wherein the first groove extends from a first surface of the compound semiconductor layer;

forming a second groove within the first groove, wherein the second groove has second sidewalls and a second lower surface;

doping the second lower surface and at least a portion of the second sidewalls with a second conductivity type dopant to form a gate region;

forming a first source region of the first conductivity type in the compound semiconductor layer adjacent to the first groove;

forming a source contact to the first source region;

forming a gate contact coupled to the gate region; and

forming a drain contact on a second surface of the compound semiconductor layer.

13. (original): The process of claim 12 wherein the step of forming the first groove includes forming the first groove in a compound semiconductor layer comprising one of GaAs and InP.

14. (original): The process of claim 12 further comprising the step of filling the second groove and at least a portion of the first groove with a passivation layer.

15. (original): The process of claim 12 wherein the step of doping the second lower surface and at least a portion of the second sidewalls includes ion implanting a second conductivity type dopant species.

16. (original): The process of claim 12 wherein the step of forming the second groove comprises the steps of:

forming spacers on the first sidewalls leaving an opening over the first lower surface; and

etching the second groove in the compound semiconductor through the opening.

17. (original): The process of claim 12 wherein the steps of forming the first and second grooves including forming

first and second grooves having substantially straight sidewall surfaces.

18. (currently amended): A method for forming a compound semiconductor FET device comprising the steps of:

providing a body of compound semiconductor material including a support wafer of a first conductivity type and a first dopant level and an epitaxial layer formed over the support wafer, wherein the epitaxial layer is of the first conductivity type and has a second dopant level lower than the first dopant level;

forming a plurality of spaced apart first doped regions of the first conductivity type in the epitaxial layer;

forming a plurality of first trenches in the epitaxial layer, wherein each first trench is between a pair of first doped regions;

forming a plurality of second trenches in the epitaxial layer, wherein one second trench is within one first trench;

doping at least portions of sidewall surfaces and lower surfaces of each second trench to form a plurality of doped gate regions, wherein the plurality of doped gate regions extend into the body of compound semiconductor material;

coupling the plurality of spaced apart first doped regions with a first contact layer;

coupling the plurality of doped gate regions to a gate connecting region; and

forming a drain contact a lower surface of the support wafer.

19. (original): The method of claim 18 of providing the body of compound semiconductor material includes providing a body of compound semiconductor material comprising one of GaAs and InP.

20. (original): The method of claim 18 wherein the step of doping the sidewall surfaces and lower surfaces includes ion implanting a dopant of the second conductivity type.